

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1192	(345/173-178).ccls.	USPAT	2001/06/05 06:23
2	BRS	L2	384	345/141.ccls.	USPAT	2001/06/05 06:24
3	BRS	L3	53	345/142.ccls.	USPAT	2001/06/05 06:24
4	BRS	L4	49	341/28.ccls.	USPAT	2001/06/05 06:25
5	BRS	L5	178	382/181.ccls.	USPAT	2001/06/05 06:25
6	BRS	L6	75	382/185.ccls.	USPAT	2001/06/05 06:26
7	BRS	L7	1903	1 or 2 or 3 or 4 or 5 or 6	USPAT	2001/06/05 06:26
8	BRS	L8	5449	(touch adj screen) or touchscreen	USPAT	2001/06/05 06:31
9	BRS	L9	3527	character adj2 process\$3	USPAT	2001/06/05 06:33
10	BRS	L10	3797	character near input	USPAT	2001/06/05 06:33
11	BRS	L11	5346	character adj2 recognition	USPAT	2001/06/05 06:34
12	BRS	L12	297525	timing or timer	USPAT	2001/06/05 06:34
13	BRS	L13	190863	expire or elapse or threshold	USPAT	2001/06/05 06:38
14	BRS	L14	1118	12 and 13 and ( 9 or 10 or 11)	USPAT	2001/06/05 06:39
15	BRS	L15	33	7 and 14	USPAT	2001/06/05 06:43
16	BRS	L16	60	"touch screen data"	USPAT	2001/06/05 06:45
17	BRS	L17	1	14 and 16	USPAT	2001/06/05 06:45



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# United States Patent [19] Shimada et al.

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## [54] ELECTRONIC DEVICE

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[\*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/173,864

[22] Filed: Dec. 23, 1993

## Related U.S. Application Data

[63] Continuation of application No. 07/790,435, Nov. 12, 1991, abandoned.

## [30] Foreign Application Priority Data

Nov. 20, 1990 [JP] Japan ..... 2,312,641

[51] Int. Cl. .... G09G 5/00

[52] U.S. Cl. .... 345/173; 345/211

[58] Field of Search ..... 345/173, 168, 345/169, 213, 211, 212, 179-183, 341/22

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### [57] ABSTRACT

An electronic device for entering information comprises a CPU for controlling the entire electronic device, information entry means for obtaining information at a predetermined time interval, and control means for controlling the CPU and the information input means such that, in a first mode in which no information is entered, the predetermined time interval is maintained in preparation for sudden entry of information and an operating clock frequency of the CPU is kept at a low frequency, and in a second mode in which information is entered, the predetermined time interval is maintained and the operating clock frequency of the CPU is kept at a high frequency.

8 Claims, 5 Drawing Sheets

